Total Charge Capacitor Model for Short-Channel MESFET's

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***Abstract*— Total charge models for short-channel metal–semiconductor field-effect transistors (MESFET's) currently available in large-signal simulator packages such as SPICE give a poor description of the bias dependence of the gate capacitance. This letter describes a novel empirical model whose structure is deduced from the reconstructed total charge function derived from measured s-parameters. The new model gives a good overall fit to the observed gate capacitance behavior of a commercial monolithic microwave/millimeter-wave integrated circuit (MMIC) MESFET over a wide range of bias conditions and enables large-signal MESFET models to have a superior fit to measured s-parameters, giving greater confidence in design.**

I. Introduction

DESIGN AND optimization of high Q active continuous time filters [1], [2] and switched capacitor filters [3] implemented in GaAs field-effect transistor (FET) technology requires accurate prediction of gate capacitance. Rodriguez [4] has shown that the capacitance models included in popular large-signal simulators do not provide an adequate fit to the gate capacitances of the equivalent circuit extracted from measured s-parameters. With frequency-selective circuits, this disparity between small- and large-signal models prevents circuits optimized with s-parameter data from being used directly with a large-signal simulator. This is overcome by lengthy and unnecessary re-optimization.

A number of capacitance models for metal–semiconductor field-effect transistors (MESFET's) have been described and can be broadly divided into three groups. Physical models require a detailed knowledge of the physical construction of the device to fit measured data. These include Takada [5], Shur [6], [7], Snowden [8]–[10], and D'Agostino [11]. There are also empirical models that describe the bias dependence of the capacitances, but these cannot readily be implemented into simulators that require total charge expressions for time domain simulation. These include Scheinberg [12], Angelov [13], and Rodriguez [4]. Finally there are the empirical total charge capacitance models that can be readily included into simulator packages, such as SPICE. These include Statz [14] and Parker [15].

Divekar [16] has suggested that the Statz model does not conserve charge. Smith [17] has explained this in terms of charge transfer between the gate-source and gate-drain ports arising from charge redistribution under the gate. Snider [18] shows how transcapacitance can achieve charge conservation at a single port of a two port capacitor. Scheinberg [19] has developed a capacitor model based on both capacitive and transcapacitve elements.

Manuscript received March 27, 1996.

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Publisher Item Identifier S 1051-8207(96)07486-7.

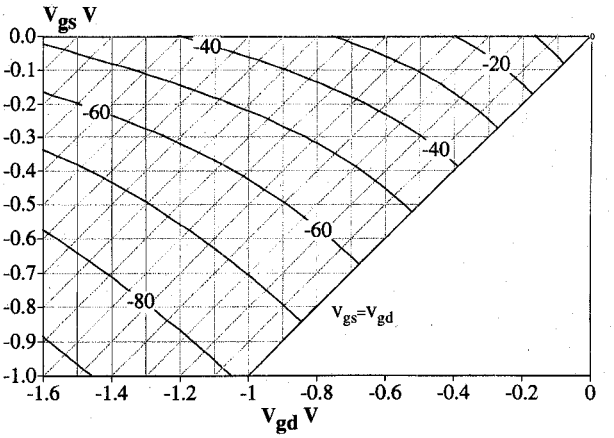

Fig. 1. Contour plot of the reconstructed Q_{gg} (fC) plotted against V_{gs} and V_{gd}.

In this letter, the authors present a new empirical total charge model that has a significantly different structure to that presented by Statz *et al.* [14] and gives a superior fit. The model is described in three parts, the overall structure, the charge-voltage relationship, and the cold FET hot FET asymmetry. Finally, the fit to the measured capacitance of a standard monolithic microwave/millimeter-wave integrated circuit (MMIC) foundry process is shown, together with a comparison to some other models.

II. Model Structure

It is possible to reconstruct the total charge behavior of a FET gate capacitance by integrating two-dimensional (2-D) bias dependant polynomial fits of parasitic gate source capacitance c_{gs} and gate drain capacitance c_{gd} with respect to their dc port voltages and combining the required terms. We show in Fig. 1. a contour plot of a reconstructed seventh-order total charge polynomial plotted against V_{gs} and V_{gd}. It can be seen that for very negative V_{gd} and $V_{gs} = 0$ (i.e., the saturated region) the curves are closely spaced together in the V_{gs} direction (corresponding to high c_{gs}) and more widely spaced in the V_{gd} direction (corresponding to low c_{gd}). About the line where $V_{gs} = V_{gd}$ (i.e. cold FET or triode region) it can be seen that the line spacing is approximately equal for both axes where c_{gs} and c_{gd} are approximately identical. Further, the curves appear to reflect in the line $V_{gs} = V_{gd}$, corresponding with the interchange of c_{gs} and c_{gd} as V_{ds} becomes negative.

This intuitively leads to a structure that can be thought of as two independent one-port capacitances whose areas are

TABLE I
MODEL PARAMETERS FOR THE L20 1 × 100 μm MESFET

$k_{sw} = 0.0372$	$c_{off} = 3.0$	$b = 2.003$
$c_{po} = 27.22$	$c_{zb} = 70.95$	$k_Q = 1.098$
$k_{Ah} = 0.1192$	$k_{Ac} = 0.9941$	$k_A = -0.2577$
$m_A = 3.159$	$v_{stc} = 0.198$	$v_{toc} = -0.4335$

modulated by an "asymmetry" function of the other port voltage. This is expressed mathematically as

$$Q_{gg}(V_{gs}, V_{gd}) = + A_{\mathrm{sym}}(V_{gs}) \cdot Q_c(V_{gd}) + A_{\mathrm{sym}}(V_{gd}) \cdot Q_C(V_{gs}) + c_{\mathrm{off}} \cdot V_{gs}. \quad (1)$$

The cold FET symmetry of the FET's depletion region necessitates that the two charge functions should be identical. This new structure is significantly different to that proposed by Statz *et al.* [14]. The c_{off} term represents a small level of asymmetry arising from crossover metallization, etc. that has not been absorbed in the extrinsic parasitic capacitances of the equivalent circuit.

III. CHARGE MODEL

Rodriguez [4] has shown that the traditional linear graded diode capacitance model gives a poor fit to observed c_{gs} behavior. The authors relax this definition and use a more general function. The structure of the function is divided into three parts: 1) a nearly constant c_{gs} below pinch off; 2) a steep rise in c_{gs} above pinchoff; and 3) followed by a more gentle slope near zero gate bias. The pinchoff voltage for the capacitance is allowed to be independent of the *I-V* behavior. The new function is described as

$$Q_C(V_x) = c_{po} \cdot (V_x - v_{toc}) \cdot (1 + k_{sw} \cdot (V_x - v_{toc})) + \frac{c_{zb} - c_{po}}{k_{c\max}} \cdot Q_D(S(V_x - v_{toc})) \quad (2a)$$

$$Q_D(V) = \left(V + \frac{V}{k_Q + V}\right)^b \quad (2b)$$

$$S(V) = v_{stc} \cdot \ln\left(\exp\left(\frac{V}{v_{stc}}\right) + 1\right) \quad (2c)$$

where c_{po} is approximately the magnitude of c_{gs} at and beyond pinchoff. c_{zb} is approximately the magnitude of c_{gs} at $V_{gs} = 0$ V in the saturated region. The coefficients b and k_d shape the slope of the c_{gs} profile with V_{gs} above pinchoff. v_{stc} controls the sharpness of the pinchoff behavior. v_{toc} is the capacitance pinchoff voltage. k_{sw} provides a first-order approximation to the sidewall behavior of c_{gd} in the saturated region, which causes c_{gd} to fall with increasing V_{ds} when V_{gd} is below the pinchoff voltage v_{toc}.

The function $S(V)$ provides a "soft turn off" for the charge function $Q_D(V)$, so that below pinchoff the capacitance is determined only by c_{po}. (This soft turn off function is also used in the Parker Skellern MESFET model [15].) The derivative of $Q_D(V)$ with the voltage v (capacitance) increases less rapidly as v increases from zero to $-v_{toc}$, giving the desired C-V behavior above pinchoff.

$k_{c\max}$ represents the change in capacitance of Q_D as V_x changes from v_{toc} to zero. $k_{c\max}$ is used to normalize the equation so that c_{po} and c_{zb} can remain fixed during optimization of the shape of the curve with b, k_d, v_{stc} and v_{toc}. $k_{c\max}$ is given by

$$k_{c\max} = \left(b + \frac{bk_Q}{(k_Q - v_{toc})^2}\right)\left(\frac{-v_{toc}}{k_Q - v_{toc}} - v_{toc}\right)^{b-1}. \quad (3)$$

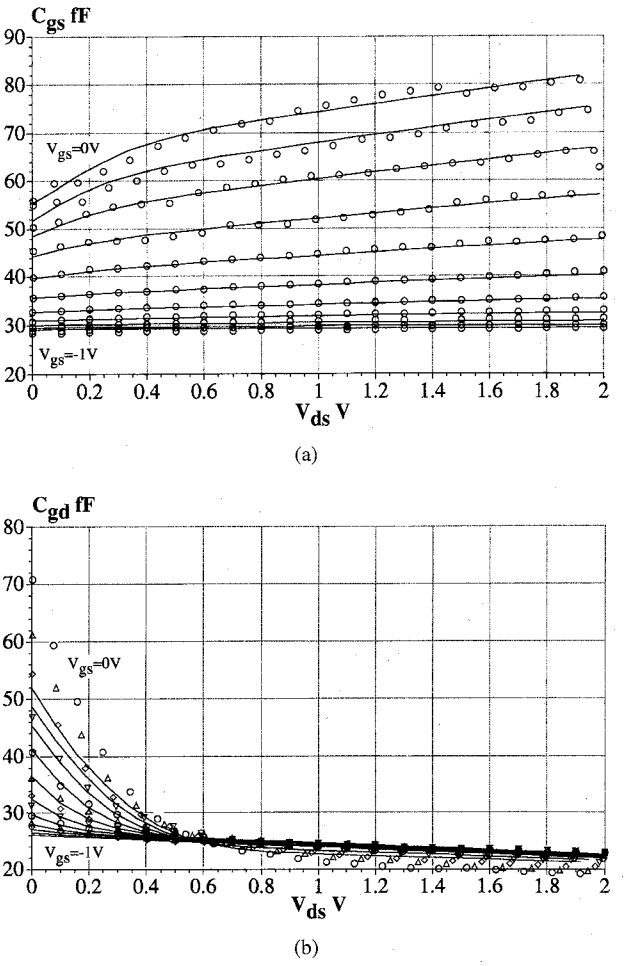

Fig. 2. Comparison of the model (line) with equivalent circuit data extracted from measured s-parameters (symbols) of a 1×100 μm L20 MESFET plotted against V_{ds} for V_{gs} from -1 V to 0 V in 0.1 V steps. (a) c_{gs}. (b) c_{gd}.

IV. ASYMMETRY MODEL

The asymmetry function is intended to force symmetry under cold FET conditions ($V_{gs} = V_{gd}$) and to enlarge c_{gs} and reduce c_{gd} in the saturated region ($V_{gs} > V_{gd}$). From equivalent circuit data extracted from measured s-parameters of two typical MESFET's, the authors observed that c_{gs} exhibits two changes in slope with respect to V_{ds}, which are most clearly seen for high V_{gs}. The first occurs near $V_{ds} = 0$, where the slope rises sharply with increasing V_{ds}. The second occurs at a higher V_{ds}, where the magnitude of the slope falls significantly. As V_{gs} becomes more negative, these changes in the slope of c_{gs} occur at lower V_{ds}, suggesting a strong V_{gd} dependence. This suggests that the asymmetry function for c_{gs} could be based on a hyperbolic tangent function of V_{gd}. The V_{gd} dependence of this transition suggests a dependence on asymmetry of the depletion region with the port voltages

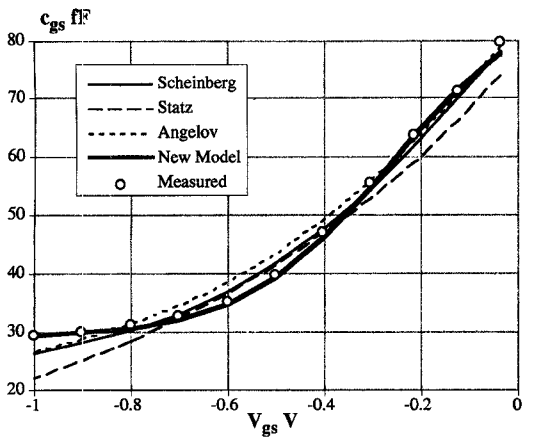

Fig. 3. Comparison of a selection of published capacitor models and the new model with the measured c_{gs} of a 1×100 μm L20 MESFET with gate bias ($V_{ds} = 1.5$ V).

rather than arising directly from velocity saturation as inferred by Statz *et al.* [14]. The asymmetry function is defined as

$$A_{\text{sym}}(V) = \frac{k_{Ac} + k_{Ah}\tanh(-m_A V + k_A)}{k_{Ac} + k_{Ah}} \tag{4}$$

where k_{Ah} and k_{Ac} determines the magnitude of the change of c_{gs} from hot to cold FET. m_A controls the position of the steep slope region of c_{gs} with V_{ds}. k_A is required to correctly center the function. The function is normalized so that changes to the shape of the cold FET region do not require c_{po} and c_{zb} to change during optimization of k_A, m_A, k_{Ah}, k_{Ac}.

V. Fit to Experimental Data

S-parameter measurements were made on a number of F20 and L20 GaAs MESFET samples from GEC Marconi Materials Ltd. Radio frequency equivalent circuits were extracted using the University of Glasgow's Lysander extraction program. The model was then fitted to the equivalent circuit data. The extracted parameters for a L20 1×100 μm FET sample are given in Table I. (The MESFET-equivalent circuit parameters Rs and Rd were constrained to be equal to their dc value and τ and R_i were set to zero, giving a good fit to the s-parameters up to 10 GHz.)

We show the fit to the L20 1×100 μm sample in Fig. 2. It can be seen that the new model gives a good fit to c_{gs} and a satisfactory fit to c_{gd} over a range of bias conditions. It correctly predicts the cross over point observed in c_{gd}, which was not predicted with the Statz model. It performs well even in the traditionally difficult area of the hot-to-cold FET transition. The model currently does not accurately predict the V_{gs} dependence of the side wall effect that is visible in c_{gd} when V_{gd} is below v_{toc}. Difficulties arise in fitting c_{gd} at low V_{ds} due to its sensitivity to the other equivalent circuit parameters during extraction from s-parameters.

In Fig. 3, a comparison is given between the models of Statz [14], Scheinberg [12], Angelov [13], and the model described in this letter. Each of the models were optimized to fit all the data of Fig. 2. A slice through c_{gs} was then taken at $V_{ds} = 1.5$ for all the models. The model of this letter offers a significant improvement in fit around pinchoff compared to the other models, which leads to a better overall fit.

Acknowledgment

The authors gratefully acknowledge the Engineering and Physical Science Research Council for support and providing access to facilities at the Rutherford Appleton Laboratory (RAL). The authors also gratefully acknowledge J. Green of GEC Marconi Materials Ltd, Caswell, U.K., for providing F20 and L20 wafers for characterization and M. Taylor of the University of Glasgow, Scotland, for providing Lysander.[1]

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[1] Lysander was supplied by M. Taylor, Dept. of Electronic & Elec. Eng., University of Glasgow, Glasgow G12 8QQ, U.K. (*User's Guide* available).